What is claimed is:

1. A checkerboard buffer page system, comprising:

a data source, providing data elements in a first order;

a data destination, receiving data elements in a second order; and

at least four memory devices, each memory device having a plurality of memory pages including a plurality of memory locations, each memory location having an address,

where data elements are stored to at least two memory devices and retrieved from at least two memory devices in parallel,

where each data element corresponds to an entry in one of a plurality of buffer pages, each buffer page having a plurality of entries along a first dimension corresponding to the first order and a plurality of entries along a second dimension corresponding to the second order,

where data elements are stored to the memory devices in the first order and retrieved from the memory devices in the second order, and where at least one memory page stores data elements in multiple locations according to the first order and stores data elements in multiple locations according to the second order,

where at least two data elements that are consecutive in the first order are stored in parallel to the memory devices, and

where at least two data elements that are consecutive in the second order are retrieved in parallel from the memory devices.

2. The checkerboard buffer page system of claim 1, where each memory page corresponds to a respective buffer page.

3. The checkerboard buffer page system of claim 1, where:

a data element is pixel data corresponding to a pixel in a frame of pixels, the frame having horizontal rows of pixels and vertical columns of pixels; and

the buffer pages are pixel pages, each pixel page having a plurality of pixel page rows and a plurality of pixel page columns.

4. The checkerboard buffer page system of claim 3, where each row of the frame includes 1920 pixels and each column of the frame includes 1080 pixels.

5. The checkerboard buffer page system of claim 3, where pixel data for two pixels is stored in parallel in one clock cycle, pixel data for one pixel to one memory device and pixel data for the other pixel to another memory device.

6. The checkerboard buffer page system of claim 3, where pixel data for two pixels is retrieved in parallel in one clock cycle, pixel data for one pixel from one memory device and pixel data for the other pixel from another memory device.

7. The checkerboard buffer page system of claim 3, where, in one clock cycle, pixel data for two pixels is retrieved from two memory devices and pixel data for two pixels is stored in two memory devices.

8. The checkerboard buffer page system of claim 7, where four memory devices are divided into a first group of two memory devices and a second group of two memory devices, and the groups alternate between storing and retrieving pixel data after storing pixel data for a frame of pixels.

9. The checkerboard buffer page system of claim 3, where pixel data is retrieved at twice or more than the rate pixel data is stored.

10. The checkerboard buffer page system of claim 9, where pixel data is stored at a rate supporting 60 frames per second, and pixel data is retrieved at a rate supporting 120 frames per second.

11. The checkerboard buffer page system of claim 9, where pixel data is retrieved for 64 pixels for every 32 pixels of pixel data that is stored.

12. The checkerboard buffer page system of claim 3, further comprising a memory controller for generating addresses for storing and retrieving data elements.

13. The checkerboard buffer page system of claim 12, where:

four memory devices are divided into a first group of two memory devices and a second group of two memory devices,

the memory controller has two states for bank alternation: a first state and a second state,

when the memory controller is operating in the first state for bank alternation, pixel data is stored to the first group of memory devices and pixel data is retrieved from the second group of memory devices, and

when the memory controller is operating in the second state for bank alternation, pixel data is retrieved from the first group of memory devices and pixel data is stored to the second group of memory devices.

14. The checkerboard buffer page system of claim 13, where the memory controller switches states for bank alternation after storing a frame of pixels.

15. The checkerboard buffer page system of claim 13, where the memory controller switches states for bank alternation based on a vertical synchronization signal.

16. The checkerboard buffer page system of claim 1, further comprising a four-by-four switch, where four memory devices are divided into a first group and a second group, each group including two memory devices, and further where the four-by-four switch provides data elements in alternation to the first group and the second group while retrieving data elements in alternation from the second group and the first group.

17. The checkerboard buffer page system of claim 1, where each memory device is an 8MB SDRAM operating at approximately 150MHz.

18. A checkerboard pixel page system, comprising:

a video source providing pixel data for pixels in a frame, the frame having rows of pixels and columns of pixels;

a video destination;

a first memory having a plurality of memory locations;

a second memory having a plurality of memory locations;

a third memory having a plurality of memory locations;

a fourth memory having a plurality of memory locations;

a memory controller connected to the first memory, the second memory, the third memory, and the fourth memory;

a first data bus connected to the video source and the memory controller;

a second data bus connected to the video source and the memory controller;

a third data bus connected to the video destination and the memory controller;

a fourth data bus connected to the video destination and the memory controller;

a source address line connected to the video source and the memory controller;

a destination address line connected to the video destination and the memory controller; and

where pixel data is stored to two memories and retrieved from two memory devices in parallel,

where each pixel corresponds to an entry in one of a plurality of pixel pages, and a pixel page includes multiple pixels from a row in the frame and multiple pixels from a column in the frame,

where each entry in a pixel page corresponds to a memory location,

where pixel data for at least two pixels that are horizontally adjacent is stored in parallel to the memories, and

where pixel data for at least two pixels that are vertically adjacent is retrieved in parallel from the memories.

19. The checkerboard pixel page system of claim 17, where the memory controller generates addresses for storing and retrieving pixel data.

20. A checkerboard pixel page system, comprising:

a video source providing pixel data for pixels in a frame, the frame having rows of pixels and columns of pixels;

a video destination;

a first memory having a plurality of memory locations;

a second memory having a plurality of memory locations;

a third memory having a plurality of memory locations;

a fourth memory having a plurality of memory locations;

a first address multiplexor connected to the first memory;

a second address multiplexor connected to the second memory;

a third address multiplexor connected to the third memory;

a fourth address multiplexor connected to the fourth memory;

a four-by-four switch connected to the first memory, the second memory, the third memory, and the fourth memory, having a first data input, a second data input, a first data output and a second data output, where the four-by-four switch switches with each frame between providing pixel data to the first memory and the second memory while receiving pixel data from the third memory and the fourth memory, and receiving pixel data from the first memory and the second memory while providing pixel data to the third memory and the fourth memory;

a source address bus connected to the video source, the first address multiplexor, the second address multiplexor, the third address multiplexor, and the fourth address multiplexor;

a first destination address bus connected to the video destination, the first address multiplexor, and the third address multiplexor;

a second destination address bus connected to the video destination, the second address multiplexor, and the fourth address multiplexor;

a first data bus connected to the video source and the four-by-four switch;

a second data bus connected to the video source and the four-by-four switch;

a third data bus connected to the video destination and the four-by-four switch; and

a fourth data bus connected to the video destination and the four-by-four switch,

where pixel data is stored to two memories and retrieved from two memories in parallel,

where each pixel corresponds to an entry in one of a plurality of pixel pages, and a pixel page includes multiple pixels from a row in the frame and multiple pixels from a column in the frame,

where each entry in a pixel page corresponds to a memory location,

where pixel data for at least two pixels that are horizontally adjacent is stored in parallel to the memories, and

where pixel data for at least two pixels that are vertically adjacent is retrieved in parallel from the memories.

21. The checkerboard pixel page system of claim 20, where the video source generates addresses for storing pixel data and the video destination generates addresses for retrieving pixel data.

22. A method of storing and retrieving pixel data, comprising:

storing pixel data for a first frame of pixels in a first memory device and a second memory device, where each memory device includes a plurality of memory pages, and at least one memory page stores pixel data for at least two pixels from each of at least two horizontal rows of pixels in the first frame of pixels;

storing pixel data for a second frame of pixels in a third memory device and a fourth memory device, where each memory device includes a plurality of memory pages, and at least one memory page stores pixel data for at least two pixels from each of at least two horizontal rows of pixels in the second frame of pixels; and

retrieving pixel data for the first frame of pixels from the first memory device and second memory device,

where pixel data for at least two pixels that are horizontally adjacent is stored in parallel to the memory devices, and

where pixel data for at least two pixels that are vertically adjacent is retrieved in parallel from the memory devices.

23. The method of claim 22, where pixel data for the second frame of pixels is stored and pixel data for the first frame of pixels is retrieved in parallel.

24. The method of claim 22, where pixel data is stored to the first memory device and the second memory device while pixel data is retrieved from the third memory device and the fourth memory device, and pixel data is retrieved from the first memory device and the second memory device while pixel data is stored to the third memory device and the fourth memory device.

25. The method of claim 22, where the memory devices switch between storing and retrieving with each frame of pixels.

26. A system for storing and retrieving pixel data, comprising:

means for storing pixel data for a first frame of pixels in a first memory device and a second memory device, where each memory device includes a plurality of memory pages, and at least one memory page stores pixel data for at least two pixels from each of at least two horizontal rows of pixels in the first frame of pixels;

means for storing pixel data for a second frame of pixels in a third memory device and a fourth memory device, where each memory device includes a plurality of memory pages, and at least one memory page stores pixel data for at least two pixels from each of at least two horizontal rows of pixels in the second frame of pixels; and

means for retrieving pixel data for the first frame of pixels from the first memory device and second memory device,

where pixel data for at least two pixels that are horizontally adjacent is stored in parallel to the memory devices, and

where pixel data for at least two pixels that are vertically adjacent is retrieved in parallel from the memory devices.